



Chip Lock Design Protection Technology

Why Chip Lock?

- **Improve product lifetime**
- **Protect your IP**
- **Protect your profits**
- **Protect your reputation**

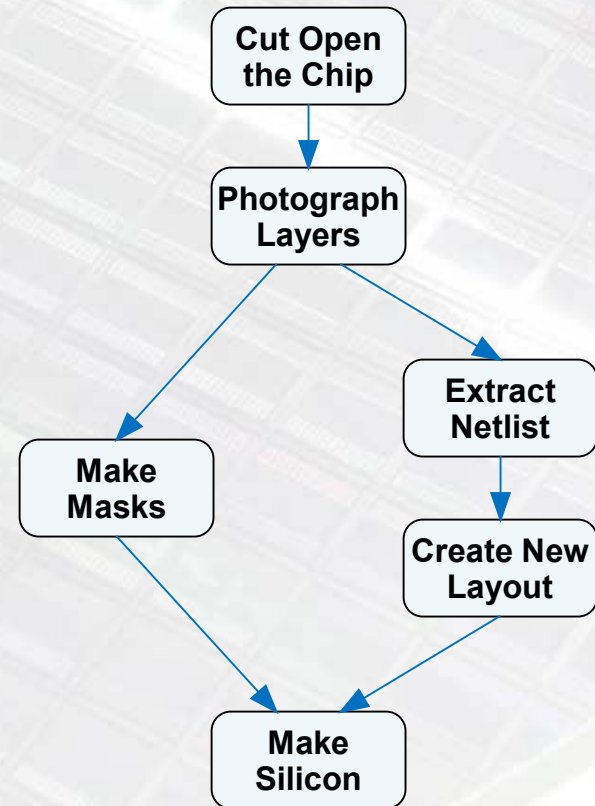
Copying Designs

2 Methods

- Copy the masks
- Copy the design

Effect of Errors

- Time > 6 months
- Cost > \$100K



Hardening The Design

Goals

- Increase the amount of work
- Increase the chances for errors



Hardening The Design

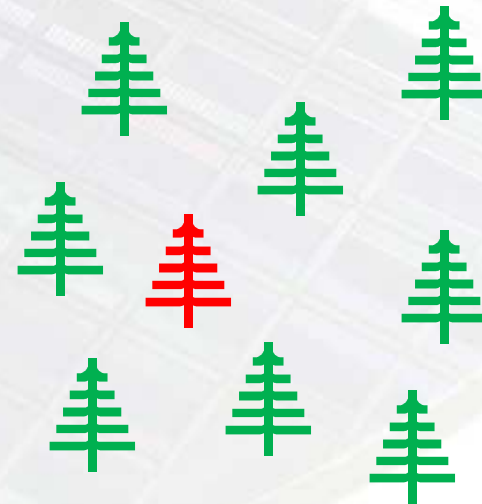
Techniques

- Adding Dummy Gates
- Adding False Interconnect
- Process Gotchas

Adding Additional Gates

Merge Dummy Chip With Original

- Increase the number of gates to analyze.
- Wastes the time of engineers.
- Does not affect original design.
- Hiding a tree by planting a forest around it.



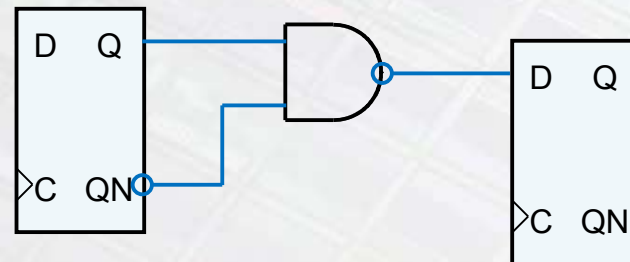
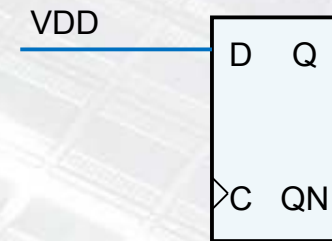
Interconnecting Additional Gates

Intermingle New Gates Through Dummy Connections

- Create nodes that are always Vdd or Vss.
- Connect them to logic nodes that are already at supply levels.

Effects

- Increases circuit complexity.
- Increases engineering time.
- Increases chances for mistakes.



Adding Additional Interconnect

Sparse Metal as Interconnect

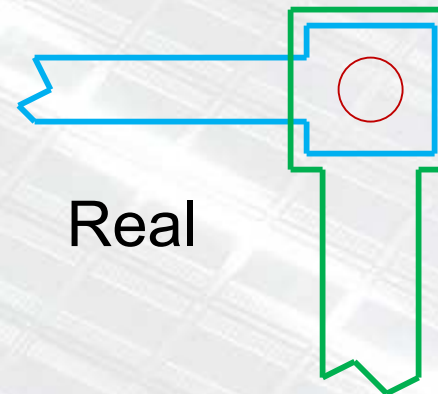
- Fab Rules Require Uniform Metal Density
- Normally Through Regular Pattern
- Use Dummy Interconnect as Pattern
- More wires to look at



Adding Real and False Vias

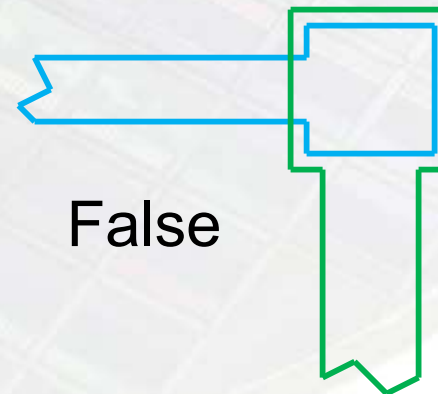
Vias Are Hard To See

- A hole in glass does not show up well.
- Identified by metal overlap



Add Real and False Vias

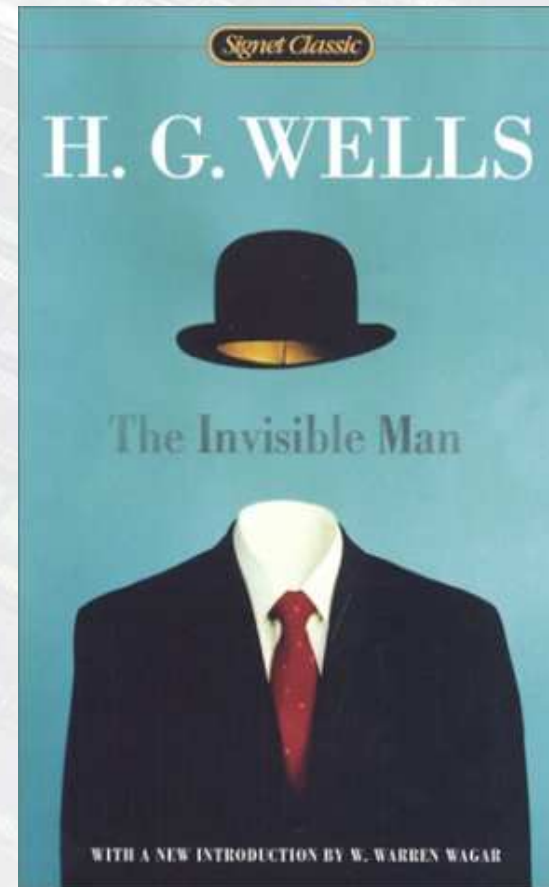
- Real Vias between dummy interconnect
- False Vias between real Interconnect
- A mistake can be fatal



Adding Process Gotchas

Invisible layers

- Implant layers are Invisible
- Use to make dead gates
- Engineer implements what he thinks that he sees, which is wrong.
- Requires customer circuit modifications



About Tekmos

- **Fabless Semiconductor Company**
 - Specialize in Obsolescence Replacement
 - Implemented Over 600 Designs Since 1997
 - Based in Austin, Texas
- **Developed 4 Key Technologies**
 - Use of Dual Oxide Fab Technologies for 5 Volt
 - Merged Designs for Low NRE and Low Volumes
 - Gate Array Approach for Both Analog and Digital
 - Stacked Die for Mixed Process Technologies
- **Used These Technologies For:**
 - Microcontrollers
 - ASICs
 - Memories
 - Standard Products



Tekmos